Docket No. 500-004

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

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| Appellant: | Chieng-Chung Chen | |
| Serial No.: | 10/696,525 | Examiner: Phan, Trong Q |
| Confirmation No: | 6390 | Group Art Unit: 2827 |
| Filing Date: | October 29, 2003 | |
| Title: | MEMORY PUMPING CIRCUIT | |

MAIL STOP APPEAL BRIEF – PATENTS
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

**RESPONSE TO NOTIFICATION OF NON-COMPLIANT APPEAL BRIEF**

Appellant submits the enclosed replacement section SUMMARY OF CLAIMED SUBJECT MATTER in response to the Notification of Non-Compliant Appeal Brief dated June 29, 2007.

V) SUMMARY OF CLAIMED SUBJECT MATTER

Appellant's claimed invention is directed to a pumping circuit (for example, the first embodiment is best depicted in Fig. 2(A), and the second embodiment is best depicted in Fig. 2(B)), which comprises a DRAM cell (21), a current source (11), and a driving circuit (13 or 22). The DRAM cell (21) is used as a charging capacitor of the pumping circuit, and includes a MOS transistor (211) and a storage capacitor (212). The DRAM cell (21) and the current source (11) are connected at a node ($V_{PP}$), which provides a pumping voltage ($V_{PP}$) as a voltage source to a memory device's word line. Specifically, in the arrangement of the DRAM cell (21), the MOS transistor (211) has a source, a drain, and a gate connected together to the node ($V_{PP}$) and to one plate of the storage capacitor (212). Another plate of the storage capacitor (212) is connected to receive the clock signal $\theta_2$ or $\alpha$ of the driving circuit (13 or 22). One primary advantage of the claimed invention, compared to the appellant's Fig. 1 Prior art or other conventional pumping circuit, is the reduced area of the charging capacitor/DRAM cell (21) required to make sure the driving current is enough for the pumping voltage ($V_{PP}$).

Independent Claim 1 recites a memory pumping circuit. The following elements are referred to, for example, Figure 2(A) or Figure 2(B) except otherwise indicated. The claimed memory pumping circuit comprises a DRAM cell 21, a current source 11, a node VPP, and a driving circuit 13 (e.g., Figure 2(A)) or 22 (e.g., Figure 2(B)). The DRAM cell 21 is used as a charging capacitor of the memory pumping circuit (see, e.g., page 4, lines 10-11 of the instant specification), and comprises a MOS transistor 211 and a storage capacitor 212 (see, e.g., page 4, lines 11-13). The current source 11 is coupled to the DRAM cell 21 for providing a charge current to the DRAM cell 21 (see, e.g., page 1, lines 17-18). The node VPP is located between the current source 11 and the DRAM cell 21 for providing a pumping voltage used as a voltage source of a word line (see, e.g., page 4, lines 17-18, and page 1, line 11). The driving circuit 13/22 generates a clock signal $\theta_2$ (e.g., Figure 2(A)) or $\alpha$ (e.g., Figure 2(B)) to drive the DRAM cell 21 (see, e.g., page 4, lines 13-15, or lines 22-25). The MOS transistor 211 has a source, a drain, and a gate connected together to the node VPP and to one plate of the storage capacitor 212,

and another plate of the storage capacitor 212 is connected to receive the clock signal $\theta_2$/ $\alpha$ of the driving circuit 13/22 (see, e.g., page 4, lines 13-15).

Independent Claim 9 recites a memory pumping circuit. The following elements are referred to, for example, Figure 2(A) or Figure 2(B) except otherwise indicated. The claimed memory pumping circuit comprises a current source 11, DRAM cell 21, and a driving circuit 13 (e.g., Figure 2(A)) or 22 (e.g., Figure 2(B)). The current source 11 is used for providing a charge current (see, e.g., page 1, lines 17-18 of the instant specification). The DRAM cell 21 is used as a charging capacitor of the pumping circuit (see, e.g., page 4, lines 10-11), and has an output port VPP for providing a pumping voltage used as a voltage source of a word line (see, e.g., page 4, lines 17-18, and page 1, line 11). The output port VPP is coupled to the current source 11 for receiving the charge current (see, e.g., page 1, lines 17-18, and page 4, lines 17-18). The DRAM cell 21 comprises a MOS transistor 211 and a storage capacitor 212 (see, e.g., page 4, lines 11-13). The driving circuit 13/22 generates a first clock signal $\theta_2$ (e.g., Figure 2(A)) or $\alpha$ (e.g., Figure 2(B)) to drive the DRAM cell 21 (see, e.g., page 4, lines 13-15, or lines 22-25). The MOS transistor 211 has a source, a drain, and a gate connected together to the output port VPP of the DRAM cell 21 and to one plate of the storage capacitor 212, and another plate of the storage capacitor 212 is connected to receive the first clock signal $\theta_2$/ $\alpha$ of the driving circuit 13/22 (see, e.g., page 4, lines 13-15).

Respectfully submitted,

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